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REMARKS/ARGUMENTS

Claims 1-21 and 29-32 are pending in the application. Claims 1, 18, 19, 21, and 29 have been amended. Support for the claims can be found in the specification as originally filed. No new matter has been introduced by virtue of these amendments.

Examiner's Response to Arguments

On page 2 of the instant Office action, the examiner has responded to arguments filed on October 25, 2006, and has requested further explanation of the difference between the claimed playback circuit as shown in Fig. 1 of the pending application and Koto's disclosed playback system. The following discussion is provided in order to respond to the examiner's request and more importantly to state for the record that the claims as previously presented are believed to be allowable over the art. However, in order to move forward with prosecution of this application, the claims have been further amended.

Throughout most of the prosecution of this case, Koto was cited for teaching a playback system. Column 6, lines 45+ had been repeatedly cited, and more recently column 10, lines 62+ have been cited. Column 10, lines 65+ describes element 200A of Fig. 1, which is "video decoding system" to be certain. Therefore, as best understood of the examiner's position, Koto's video decoding system 200A teaches a playback system.

However, according to Koto, "FIG. 1 shows ... a video coding/decoding system ... according to the first embodiment... ." Therefore in addition to showing a playback system (i.e., video decoder 200A), Fig. 1 of Koto, also shows a "video coding system 100A" which is discussed in column 9, lines 56+. Throughout most of the prosecution, Fig. 7 had been cited for teaching many of the recited claim elements. Fig. 7, however, is detail about the video coding system 100A. It is an improper reading of Koto's Fig. 1 to say that the entirety of the figure teaches a playback system. This is simply not the case.

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As to Fig. 1 of the pending application, the examiner's explanation is excerpted:

information to playing back the data that is processed into the system. Furthermore, it

is noted that the playback circuitry disclosed by Koto is similar to the present application

Figure 1 wherein various part (i.e., watermark detector, decoder, playback circuits) all

make up the entire system for reproducing, recording and playing back information.

Fig. 1 of the pending application in its entirety shows a reproduction circuit. To be sure, the present invention can be embodied in a device that provides recording as well as playback (e.g., see page 4, lines 23+). However, first and foremost, Fig. 1 shows only the playback component (e.g., see page 3, lines 14+ and page 4, lines 5-6). The examiner's comment, indicates she may have missed this subtle point, and the undersigned offers his apologies for not realizing this earlier and clarifying it for the examiner. Therefore, contrary to the examiner's understanding, Applicant's Fig. 1 does not "make up the entire system for reproducing, recording and playing back information." Applicant's Fig. 1 does not show any "recording" components, they are all related to playback.

It is hoped that with this understanding, the examiner will be persuaded that the previous reliance on Fig. 7 of Koto is improper because Fig. 7 of Koto relates to specifics of a video coding system 100A (a recording circuit), while the pending claims (as illustrated in Applicant's Fig. 1) are directed to a playback circuit.

Embodiments of the Present Invention

Embodiments in accordance with the present invention detect a watermark embedded in data by storing a portion of that data including the watermark in a buffer memory and using a watermark detection module to detect the watermark. An illustrative embodiment is shown in Fig. 1 (reproduced below):

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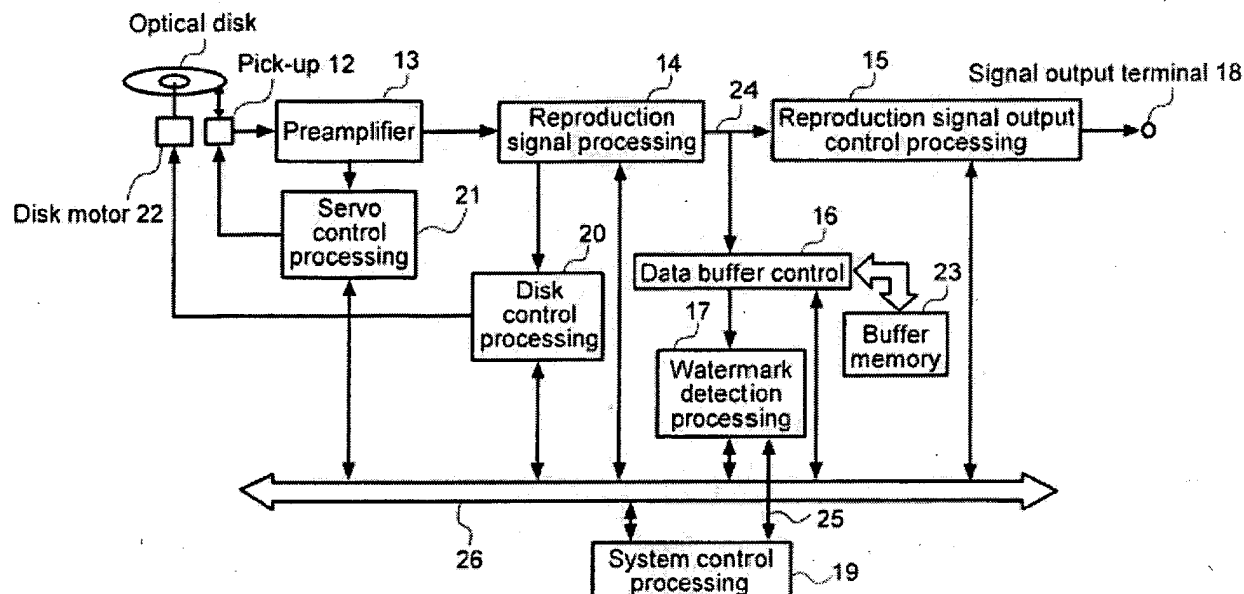
[A] predetermined amount of data required for watermark detection is written to the buffer memory . . . [t]he watermark detection processing block 17 does not need to detect watermarks directly from data 24 having a high data transfer rate by carrying out watermark detection processing on data stored in the buffer memory and may detect watermarks from the data stored in the buffer memory 23, thereby eliminating a restriction on detection speed (emphasis added). *See page 9, lines 33-34; page 8, lines 15-19 of the present specification.*

Accordingly, independent claim 1 recites in part as follows:

1.   An apparatus for playing back data stored on an information recording medium, the data having audio information, visual information, or audio-visual information, the data containing a watermark, the apparatus comprising:

a reproduction processing circuit configured to receive the information that is stored on the information recording medium to produce the data; and

playback circuitry comprising:

a data store;

a data selection circuit configured to select a subset of the data which is necessary for the detection of the watermark and to store the subset of the data into the data store;

a detecting circuit coupled to the data store and configured to process data contained therein to produce a detection result, the detection result being based on the watermark . . .

a control circuit configured to selectively output the data based on the detection result,

wherein the data selection circuit and the detecting circuit operate in alternating fashion to alternate between storing a subset of the data to the data store and reading out the subset of the data for watermark detection. (underlining added for emphasis)

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The other pending independent claims recite similar features. The data selection circuit as claimed selects a portion (i.e., subset) of the data containing a watermark and stores that portion in a buffer memory. The detecting circuit processes the portion in the buffer memory to detect the watermark. The watermark may contain a control code that prohibits or permits the reproduction of data. The control circuit selectively outputs the data based on this control code. *See, e.g., page 8, lines 3-10 of the present specification.*

Section 103 Rejection of Claims 1, 7-12, 14-15, 18-19, 20-21, and 31-32

Claims 1, 7-12, 14-15, 18-19, 20-21, and 31-32 were rejected under 35 U.S.C. §103(a) as being unpatentable over Koto et al. (U.S. Patent No. 6,671,376) in view of Copeland et al. (U.S. Patent No. 5,659,613). These claim rejections are overcome as follows.

The Koto reference is directed to a video decoding system that detects embedded watermark signals in a video signal. The decoder 200A component shown in Fig. 1 of Koto is reproduced below, along with a discussion of playback processing:

200A
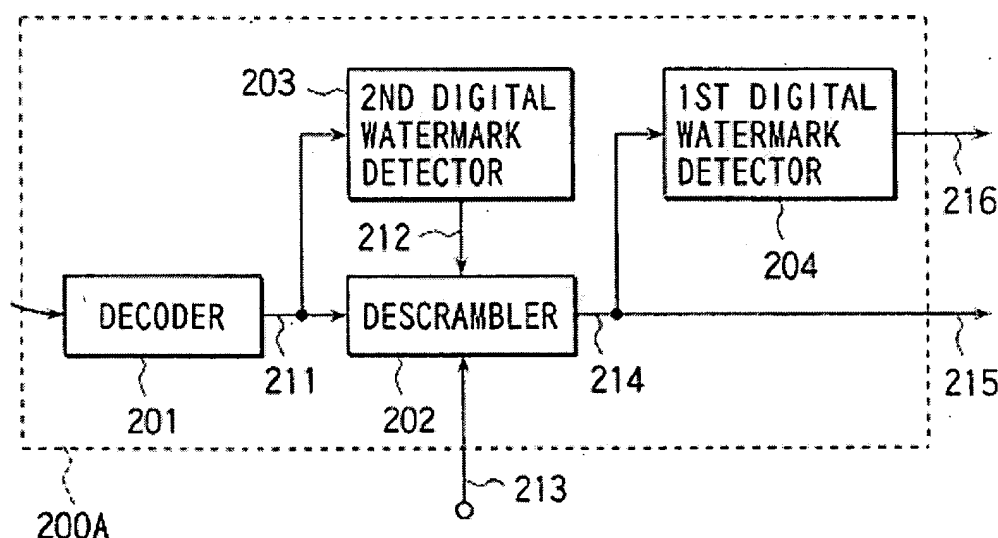
When information such as copyright information, playback control information, or the like is multiplexed as a digital watermark on the video signal 214, <u>the video signal 214 is input to the digital watermark detector 204</u> corresponding to the first digital watermark detector 102, and digital watermark information 216 is output (underlining added for emphasis; column 10, line 64 to column 11, line 3 of Koto).

Video signal 211 is a scrambled signal to be descrambled by descrambler 202. Second digital watermark detector 203 detects scramble key information 212 from scrambled

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video signal 211. Descrambler 202 reconstructs a descramble key based on scramble key information 212. First digital watermark detector 204 takes "the video signal 214" as an input and outputs digital watermark information 216 (see column 10, lines 43-48 of Koto).

The Koto Reference Does Not Teach or Suggest the Claimed Data Selection Circuit

The Koto reference simply describes reference numbers 211, 203, and 212 working together as a descrambling module. The above-cited text of Koto (i.e., *the video signal 214 is input to the digital watermark detector 204*) suggests that the entire video signal is input to the digital watermark detector; there is no suggestion whatsoever, that only a portion of the video signal is input to the detector 204. Thus, Koto teaches a detection circuit, i.e., his watermark detector 204. Koto is completely silent as to the claimed data selection circuit, where the data selection circuit as recited selects a subset of the data and stores the subset of the data in a buffer memory. The Koto reference fails to teach or suggest this feature of the present invention.

The Koto Reference Does Not Teach or Suggest the Claimed Detecting Circuit

Koto teaches a watermark detector 204. However, without any mention of inputting a portion of the data to the digital watermark detector, the Koto reference fails to teach or suggest that the digital watermark detector processes only a specific subset of data containing the watermark. In comparison, the claimed detecting circuit processes data stored in the buffer memory (i.e., the portion of data containing the watermark) to produce a detection result, such as detecting the watermark. The claimed detecting circuit is different from Koto's watermark detector because the claimed detecting circuit is given a specific portion of data to process, whereas Koto's watermark detector, as best understood, is given the entire data stream to process. Koto's watermark detector 204 does not anticipate the recited "detecting circuit coupled to the data store and configured to process data contained therein to produce a detection result" where the data store stores a subset of the data obtained from the information recording medium.

The Koto Reference Does Not Teach or Suggest the Claimed Control Circuit

The Koto reference further fails to teach or suggest "selectively outputting the data" as recited in the claimed control circuit. Referring to column 10, lines 62-64 of Koto, the

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video signal descrambled by the descrambler is <u>output as an output signal</u> to be output to a video display device or recording device. The Koto reference is silent as to describing any selective control of the data output; i.e., prohibiting or permitting. As best understood, Koto's descrambler <u>always outputs</u> an output signal, irrespective of whether the proper descramble code is present. Without any mention of control codes or any other means of controlling the output of data, in no way would one of ordinary skill understand Koto's descrambler to teach selectively outputting the data.

The Koto Reference Does Not Teach or Suggest Alternating Between Storing and Reading

It follows from the above that the Koto reference also does not teach:

"wherein the data selection circuit and the detecting circuit operate in alternating fashion to <u>alternate between storing</u> a subset of the data to the data store <u>and reading out</u> the subset of the data for watermark detection" (underlining added for emphasis)

as recited in the independent claims. This feature describes how the data selection circuit and detecting circuit operate when detecting watermarks. Because the Koto reference does not teach the claimed data selection circuit and the claimed detecting circuit, the Koto reference *ipso facto* cannot legitimately be understood as teaching the "alternating fashion" recited in the pending claims.

The Copeland Reference Does Not Teach or Suggest the Features of the Claimed Invention

The Copeland reference fails to overcome the deficiencies of the Koto reference. The Copeland reference is directed to detecting a video finger print signal inserted into a video signal prior to MPEG encoding. The video finger print detector generates a copy protection signal which is coupled to a first input of an AND gate. *See FIG. 2 and column 6, line 61 to column 7, line 7 of Copeland.*

While the Copeland reference discloses detecting a video finger print signal, the Copeland reference does not teach or suggest the above-cited features of the data selection circuit of the present invention. Specifically, referring to column 6, lines 63-64 of Copeland, the finger print detector "<u>continuously stores</u> field one and then subtracts it from field two of <u>each frame</u>" (emphasis added). Here, the reference suggests that the finger print detector processes each frame (i.e., the entire video signal). The Copeland reference is silent as to suggesting that only a

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portion of the video signal is processed by the video finger print detector. Without such teaching, in no way can Copeland's video finger print detector be understood as the claimed data selection circuit.

Based upon the failure of the Koto and Copeland references to teach or even suggest each of the elements of the pending claims, it is respectfully asserted that claims 1, 7-12, 14-15, 18-19, 20-21, and 31-32 are patentable. The Section 103 rejection of the claims is believed to be overcome.

Section 103 Rejection of Claims 8-12

Claims 8-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yamagata et al. (U.S. Patent No. 5,956,460) in view of Copeland et al. These claim rejections are overcome as follows.

The Yamagata reference is directed to a reproducing apparatus for reproducing audio and video signals. A discrimination circuit is arranged in combination with a reproduced RF signal detection circuit to demodulate a reproduced RF signal and to discriminate the recorded signal between a video signal and an audio signal (column 3, lines 8-12 of Yamagata). While the Yamagata reference relates to processing video and audio signals, the Yamagata reference lacks any teaching as to detecting watermarks embedded in the video/audio data. Specifically, there is no mention of the discrimination circuit detecting watermarks in the video/audio data. Moreover, the discrimination circuit does not take a portion of the data and store that portion in a buffer memory. Without the description of these features of the data selection circuit of the present invention, Yamagata's discrimination circuit cannot be understood as the claimed data selection circuit.

As stated above, the Copeland reference also does not teach or suggest the claimed data selection circuit. Thus, the combination of the Yamagata and Copeland references fails to teach or even suggest each of the elements of the pending claims. As such, it is respectfully asserted that claims 8-12 are patentable. The Section 103 rejection of the claims is believed to be overcome.

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Section 103 Rejection of Claims 2-6 and 13

Claims 2-6 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Koto et al. in view of Copeland et al. in further view of Fujinami et al. (U.S. Patent No. 6,192,189). These claim rejections are overcome as follows.

The Fujinami reference fails to overcome the deficiencies of the Koto and Copeland references. The Fujinami reference is directed to a data decoding apparatus that separates portions of speech/video data to be reproduced. Fig. 12 of the Fujinami reference is reproduced in part below, along with relevant text:
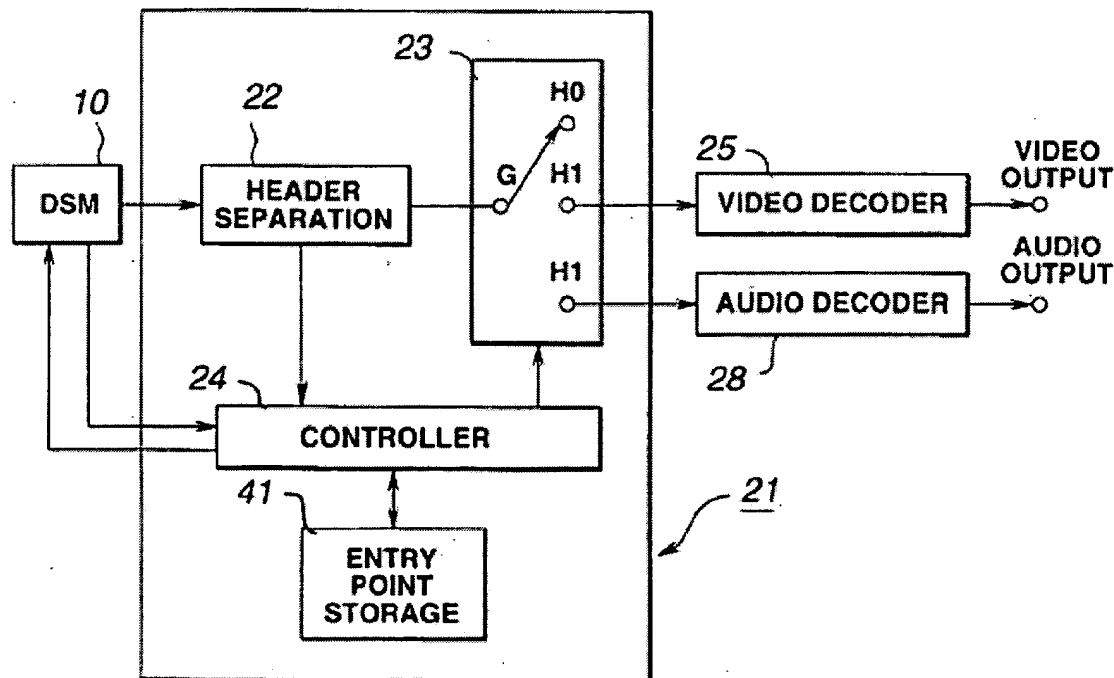
A header separation circuit 22 of the separation device 21 separates a pack header, a sector header, and an entry sector from data read out from the DSM 10 and routes the separated data to a controller 24, while routing time-divisional multiplexed data to an input terminal G of a switching circuit 23. The switching circuit 23 has its output terminals connected to an input terminal of an audio decoder . . . With the present decoding apparatus for the multiplexed data, the controller 24 controls the reproducing operation so that it selects an audio stream by the path designated by the path designation signal as set by the user and the information on the path of the multiplexed bitstream for causing audio data matched to the video data to be decoded by the audio decoder (underlining added for emphasis; column 10, lines 56-63; column 11, lines 18-24 of Fujinami).

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Here, the Fujinami reference describes the separation device as a de-multiplexer. The audio/video data from data source DSM is separated based on a path designated by the user. The audio data is matched with its corresponding video data.

The Fujinami reference does not teach or suggest that the separation device selectively outputs the data as recited in the claimed control circuit, it separates the data into audio data and video data. The switching circuit is shown to route video and audio data to the video decoder and audio decoder, respectively. The Fujinami reference is silent as to describing selectively prohibiting the output of data. One is led to believe that Fujinami's switching circuit always outputs an output signal. Without any mention of control codes or any other means of controlling the output of data, in no way can one find Fujinami's switching circuit as selectively outputting the data.

Furthermore, while the Fujinami reference discloses dividing video/speech data into packets, the Fujinami reference lacks the teaching of storing these packets into a buffer memory, and detecting a watermark found within these packets. In fact, there is no description of watermark detection in the entire reference. Without such reference to watermark detection, the Fujinami reference cannot suggest the claimed data selection circuit.

Based upon the failure of the Koto, Copeland, and Fujinami references to teach or even suggest each of the elements of the pending claims, it is respectfully asserted that claims 2-6 and 13 are patentable. The Section 103 rejection of the claims is believed to be overcome.

## Section 103 Rejection of Claims 16 and 17

Claims 16 and 17 were rejected under 35 U.S.C. §103(a) as being unpatentable over Koto et al. in view of Copeland et al. in further view of Yamagata et al. As stated above, the Koto, Copeland, and Yamagata references fail to teach the claimed data selection circuit of the present invention.

Based upon the failure of the Koto, Copeland, and Yamagata references to teach or even suggest each of the elements of the pending claims, it is respectfully asserted that claims 16 and 17 are patentable. The Section 103 rejection of the claims is believed to be overcome.

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Section 103 Rejection of Claim 29

Claim 29 was rejected under 35 U.S.C. §103(a) as being unpatentable over Koto et al. in view of Copeland et al. in further view of Hashimoto (U.S. Patent No. 6,826,289).

The Hashimoto reference fails to overcome the deficiencies of the Koto and Copeland references. Specifically, the Hashimoto reference does not teach or suggest a watermark detector coupled to a buffer memory, where only a portion of data is stored in the buffer memory and the watermark detector processes the portion of the data to detect the watermark. Fig 2 of the Hashimoto reference is reproduced in part below:
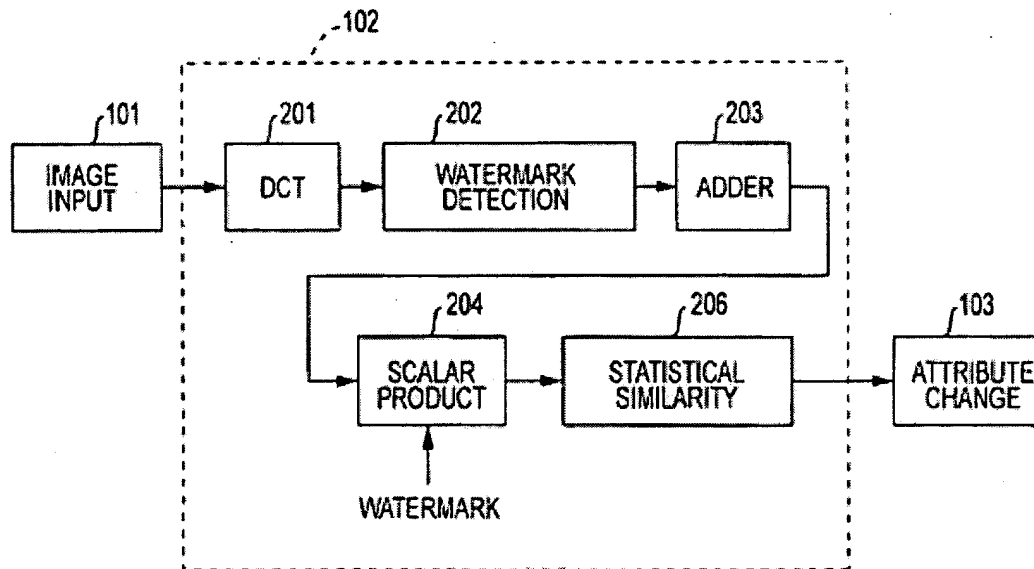
The inputted image is transformed by DCT means 201 to extract an estimation value of the embedded electronic watermark data in frequency space by using electronic watermark detection means 202. Then, the statistical similarities between known electronic watermarks and the extracted watermark data are calculated. Thus, attribute detection result 103 of the inputted image is obtained (underlining added for emphasis; column 5, lines 5-12 of Hashimoto).

In the latest office action, the Examiner refers to Hashimoto's watermark detection means 202 as teaching the claimed detecting circuit. While the Hashimoto reference discloses extracting an "estimation value" corresponding to extracted watermark data, this estimation value is not a subset of the image input data.

Hashimoto's watermark detection means obtains attribute information of the image data. The extracted estimation value corresponds to this attribute information, such as

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brightness, color, etc. (see, e.g., column 5, lines 10-19 of Hashimoto). However, the Hashimoto reference is silent as to mentioning that the estimation value is actually a subset of the image data. Without such teaching of processing a portion of the image data, in no way can Hashimoto's watermark detection means be understood as the claimed detecting circuit.

Moreover, the Hashimoto reference does not teach the claimed control circuit. Referring to Fig. 3 of Hashimoto, an image output apparatus is connected to a brightness register and an adder. The image output apparatus displays the image data based on the attribute data. The Hashimoto reference is silent as to describing any control of this data output. Without any mention of control codes or any other means of controlling the output of data, in no way can one find Hashimoto's output apparatus as selectively outputting the data.
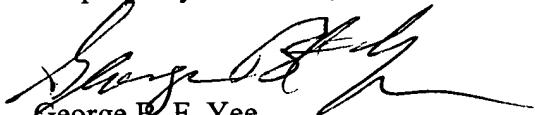
Based upon the failure of the Koto, Copeland, and Hashimoto references to teach or even suggest each of the elements of the pending claims, it is respectfully asserted that claim 29 is patentable. The Section 103 rejection of the claims is believed to be overcome.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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